Remarks

Applicant respectfully requests reconsideration of this application. Applicant has amended claims 1 & 24; not substantively, but rather to merely make explicit what was implicit or inherent in the claims as originally filed. As such, Applicant believes that claims 1 & 24 should be entitled to a full range of equivalents. Claim 16 has been amended to more distinctly claim the present invention. Claim 23 has been canceled. No claims have been allowed.

Claim Rejection - 35 U.S.C. § 103(a)

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takiguchi (US 5,986,463; "Takiguchi"). Additionally, claims 5-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takiguchi in view of Lajolo (US Patent Publication No. 2002/0188892; "Lajolo").

Takiguchi teaches a differential signal generating circuit 16 that includes a plurality of inverters coupled to drive a differential switch 18a buffer in a logic circuit. The differential signal generating circuit 16 improves the problem inherent in the prior art; namely, the simultaneous deenergization of the transistors MP4 and MP5 of the differential switch. The solution taught by Takiguchi provides for small signal amplitudes input to the gates of transistors MP4 and MP5 in order to suppress the noise level of radiation due to variation in the gate potential (at transistors MP4 and MP5) leaked to the output terminals IO and ION. (See Figure 8a; column 10, lines 17-26). This type of gate-to-source noise leakage is distinguished from the crosstalk-induced noise suppression that is the aim of the present invention. Nowhere does Takiguchi mention crosstalk, or crosstalk-induced noise. This is understandable since Takiguchi is directed to solving the problem of deenergizing the differential output transistors of a switch operated at high frequency, which problem does not involve crosstalk. In other words, the object or purpose of

Takiguchi's differential signal generating circuit is very different than that of the claimed invention.

Takiguchi's differential signal generating circuit includes an inverter circuit group 15 that consists of three inverters coupled in series between input and output nodes, with two intermediate nodes of the inverter circuit group driving first and second pseudo-inverters 13 & 14. Pseudo-inverters 13 & 14 generate a complementary output logic signal. (See Figs. 1-2; col. 6, lines 22-63) The relative sizes of Takiguchi's three inverter stages, 21, 31, and 41 are 1, 2, and 3, respectively. (Col. 9, lines 52-65; col. 1, lines 26-39) Thus, Takiguchi fails to teach first and second inverters connected in series between input and output nodes, with the second inverter having a device size at least six times greater than that of the first inverter, as recited in amended claim 1.

By disclosing an inverter circuit group with three inverter stages (as sized above) Takiguchi actually teaches away from the two inverter stage buffer approach of the claimed invention. For example, with respect to his prior art Figures 9(a) & 9(b), Takiguchi describes setting a relatively narrow channel width of each of the p- and n-channel MOS transistors in an attempt to slow down the rise and hasten the fall of the inverters 22 & 23. But according to Takiguchi, although this approach shows some improvement, the current spike L at the output terminal still has a large value. (Col. 1, line 52 through col. 4, line 5) As a result, Takiguchi's solution eschews the two inverter approach in favor of his three inverter circuit group 15 coupled with his first and second pseudo-inverters 13 and 14.

The Federal Circuit has noted that one important indicia of non-obviousness is "teaching away" from the claimed invention by the prior art. *In re Dow Chemical Co.*, 837 F.2d 469, 473 (Fed. Cir. 1988); see also, *In re Haruna*, 249 F.3d 1327, 1335 (Fed. Cir. 2001) In this case, Applicant respectfully submits that a skilled artisan would definitely have been discouraged from attempting the invention of

claims 1-4 since Takiguchi teaches away from a two inverter stage buffer approach.

Furthermore, Takiguchi fails to teach, disclose, or suggest any approach – e.g., either two or three inverter stages – in which the relative inverter size difference between the inverter connected to the output node is at least six times greater than the size of the inverter connected to the input node. In other words, Takiguchi fails to teach or suggest Applicant's noise suppression buffer recited in amended claim 1.

Even though the Examiner considers that such an inverter size difference would have been obvious "in order to meet design requirement" there is nothing in the prior art that suggests an ordinary practitioner would have been motivated to design a two inverter stage buffer for noise reduction purposes, wherein the second inverter is at least six times greater in size as compared to the first inverter. "The mere fact that the prior art may be modified in a manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14 (Fed. Cir. 1992) *citing In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984) Consequently, Applicant respectfully submits that the subject matter of claims 1-4 would not have been obvious to one of ordinary skill at the time it was made in view of Takiguchi. That is, applicant respectfully submits that there is nothing in the Takiguchi reference which would have motivated an ordinary practitioner in the art to implement Applicant's noise reduction buffer of amended claim 1.

As to independent claims 5 and 16, Marcell teaches a system-level methodology together with a distributed bus guardian architecture in which dedicated hardware modules constantly monitor the bus in order to detect bus errors (arising from crosstalk) as soon as they appear. Whenever possible, Marcell's bus guardian architecture attempts to restore the correct logical value on the bus line.

Marcell, however, fails to teach "extracting parametric information from a layout of the logic network", and "analyzing the logic network to identify a crosstalk-

induced glitch at a node of a signal path in the logic network" as per claim 5. Similarly, Marcell fails to disclose "identifying a crosstalk-induced glitch at an input node of a logic state device in a signal path of the logic network", "determining a timing slack figure at the input node", and "inserting a buffer in the signal path at the input node so as to suppress the magnitude of the crosstalk-induced glitch ... ", as per amended claim 16. On the contrary, paragraphs 0028-0029 of Marcell (specifically identified in the office action) merely describe results obtained for a specific bus implementation, which results have been charted in order to "extract the probability of error due to crosstalk given the length of the wires and the frequency of the signal injected on active line 10."

In other words, rather than extracting parametric information (e.g., capacitance, resistance, etc.) from logic circuit layout and then using that information to insert a specialized buffer at a certain node in the signal path, the representations of Figures 2 & 3 in Marcell are used for the purpose of *predicting* the likelihood of an error due to crosstalk so that safe layout rules (such as "carefully choosing distance D" between bus guardians) can be adopted. To put it differently, the object of Marcell's invention is not to suppress crosstalk induced noise. Rather, his object is provide a methodology for locating the bus guardians based on statistical probabilities (at the system behavioral level), and then rely on his bus guardians to detect when a glitch actually occurs in the physical circuit, and, if possible, correct the bus error.

According to Marcell, coarse floorplanning and chip characterization parameters (such as design rules, levels of metal, power supply voltage, etc.) are provided to a user in order to extract his all- important statistical probability of the occurrence of single and double bus wire faults. (See paragraphs 0059-0060). In contrast, the invention of independent claims 5, 16 and 24 does not rely upon statistical probabilities or the sort of high-level chip characterization parameters

utilized in Marcell's methodology. That being the case, there is no disclosure, teaching, or suggestion in Marcell of a computer-implemented method comprising extracting parametric information from a layout of the logic network, analyzing the logic network to identify a crosstalk-induced glitch at a node of a signal path in the logic network, and inserting a buffer at the node that functions to suppress a magnitude of the crosstalk-induced glitch, as recited in representative claim 5. The same is true with respect to Applicant's independent claims 16 & 24.

Because the Marcell and Takiguchi references do not teach or suggest the elements recited in claims 5-29, it is respectfully submitted that the rejection of claims 5-29 does not satisfy the criteria to establish *prima facie* obviousness. Even if the references teach what the Examiner says they teach, there still is no suggestion, teaching, or motivation to combine Takiguchi with Marcell in the manner suggested by the Examiner, or to modify these references in any manner, to arrive at the claimed invention. The recited claim elements are simply not disclosed in or suggested by any of the cited prior art references, or their combination. Therefore, the inventions of pending claims 1-29 would not have been obvious to a person of ordinary skill in the art at the time the invention was made in view of the prior art.

Accordingly, it is respectfully submitted that all pending claims are now in condition for allowance.

Please charge any shortages and credit any overcharges to our Deposit Account No. 50-2060.

Respectfully submitted,
BURGESS & BEREZNAK, LLP

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(37 C.F.R. § 1.8(a))

I hereby certify that the foregoing **Amendment and Response** is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the M/S Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 4, 2005.

Bradley Bereznak
Name of Person Mailing Correspondence

Signature

April 4, 2005
Date